We Claim:

1. A configuration for checking an address generator of a test apparatus of an integrated circuit, comprising:

an address bus having lines;

a set of first switching devices connected to said lines and to the address generator, the address generator having a given number of address outputs connected by said set of first switching devices to said lines of said address bus for outputting first address values, generated in the address generator, onto said address bus;

a set of second switching devices connected to said lines;

at least one access point; and

a memory apparatus with a plurality of memory elements equal to the given number of address outputs of the address generator and connected to said set of second switching devices, said memory apparatus receiving an external address signal for storing second address values, and the second address values stored in said memory apparatus being output from said memory elements of said memory apparatus onto said lines of said address bus through said set of second switching devices, said memory apparatus storing values of address

signals present on said lines of said address bus, said memory apparatus connected to said access point and the values stored being output by said memory apparatus to said access point.

2. The configuration according to claim 1, further comprising a control device for controlling storage of the values of the address signals present on said lines of said address bus into said memory apparatus.

3. The configuration according to claim 1, further comprising at least one third switching device connected between said memory apparatus and said access point for outputting the values of the address signals stored in said memory apparatus to said access point.

4. The configuration according to claim 1, wherein the values stored in said memory apparatus are output serially to said access point.

5. The configuration according to claim 1, wherein said access point is one of a plurality of access points coupled to said memory apparatus, and the values stored in said memory apparatus are output in parallel to said access points.

6. A method for checking an address generator of a test apparatus of an integrated semiconductor circuit, which comprises the steps of:

generating address signals in the address generator;

outputting the address signals output onto lines of an address bus;

transferring the address signals present on the lines of the address bus to a memory apparatus; and

forwarding the address signals from the memory apparatus to at least one access point.

7. The method according to claim 6, which further comprises outputting serially the address signals to the access point.

8. The method according to claim 6, which further comprises outputting in parallel the address signals to a plurality of access points.

9. The method according to claim 6, which further comprises carrying out the checking during a special test mode of the integrated semiconductor circuit.

10. A method for checking an address generator of a test apparatus of an integrated circuit, which comprises the steps of:

generating address signals in the address generator;

outputting the address signals through a set of first switching devices onto lines of an address bus;

transferring the address signals present on the lines of the address bus through a set of second switching devices to a memory apparatus being part of the test apparatus; and

outputting the address signals from the memory apparatus to at least one access point.